Pergamon

Int. J. Heat Mass Transfer. Vol. 41, No. 11, pp. 1549–1557, 1998

Printed in Great Britain
0017–9310/98 $19.00+0.00

PII: S0017–9310(97)00207–X

Transient heat transfer in batch thermal reactors for silicon wafer processing

YONG-HUI FAN and TAIQING QIU†

Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139, U.S.A.

(*Received* 19 *January* 1997 *and in final form* 7 *July* 1997)

Abstract—Precise thermal control of multi-zone batch furnaces has become increasingly important in semiconductor industry to prevent defect generation during device fabrication. This work analyzes fundamental heat transfer processes during fast furnace ramping. Model simulations show two significant thermal features: (1) the radial temperature distribution on wafers follows a universal parabolic profile; and (2) a wafer stack produces a strong cavity effect for thermal radiation. An engineering model is developed based on these features to characterize the dependence of wafer temperature nonuniformity on processing conditions, including the ramp rate and wafer spacing. This simple yet accurate model is useful for real-time process control.

INTRODUCTION

Multi-zone batch furnaces have been widely used for front-end-of-line fabrication of integrated circuits, including oxidation, implant activation, annealing, alloying, and CVD deposition. Such thermal reactors are generally heated by external resistance heaters wrapped around a quartz process tube. The substrate wafers are stacked concentrically inside the process tube and heated up from a push temperature to a prescribed process temperature. After predefined process results are achieved, the wafers are cooled down from the process temperature to a pull temperature. During these heating and cooling processes, temperature nonuniformity develops on the wafer surfaces due to a nonuniform distribution of view factors from different regions of the wafers to the heating or cooling environment. The radial wafer temperature distribution produces thermal stresses which can exceed the yield strength of the material, causing plastic deformation. As the critical device dimensions in VLSI/ULSI circuits continue to shrink and the wafer size continues to increase, tighter control of thermal budget (time of wafer exposure to a high temperature environment) and temperature nonuniformity has become a challenging issue. While fast temperature ramps can reduce thermal budget of wafers, large ramp rates tend to increase temperature nonuniformity which in turn induces large thermal stresses. A better understanding of the thermal characteristics of batch furnaces is necessary.

Hu studied transient cooling of wafers when they are quickly brought out of a high-temperature furnace into a room-temperature ambient [1]. Mokuya *et al.* investigated transient wafer temperature distribution during wafer insertion and withdrawal [2, 3]. Van Schravendijk and De Koning simulated wafer temperatures when room-temperature wafers were suddenly exposed to a 1000 K furnace tube [4]. Tavel and Hearn developed a computer model to describe thermal cycling of wafers [5]. Fan and Qiu analyzed thermal and mechanical behaviors of silicon wafers during ramping processes and proposed a temperature control scheme to achieve fastest ramps of batch thermal reactors [6]. These models, however, require sophisticated numerical solutions and cannot be applied for real-time process control.

The objective of this work is to develop a simple yet accurate thermal model for furnace design and process control. A general thermal radiation and heat conduction model is first presented and then employed to characterize fundamental thermal features of silicon wafers during rapid furnace ramping. These features are utilized to simplify a wafer stack as a cylindrical surface of an effective emissivity and an apparent temperature. Direct relationships between the furnace heater temperature, averaged wafer temperature and wafer-temperature uniformity are established.

HEAT TRANSFER IN A BATCH THERMAL REACTOR

A batch thermal reactor consists of three key elements: a stack of wafers, electrical resistive heaters, and a fused-silica process tube [Fig. 1(a)]. For the majority of batch reactor applications like oxidation and CVD deposition, the two surfaces of a silicon wafer have the same emissivity and thus the same surface radiative heat flux. The wafer stack can be represented by a unit cell formed by two adjacent

† Author to whom correspondence should be addressed.

NOMENCLATURE

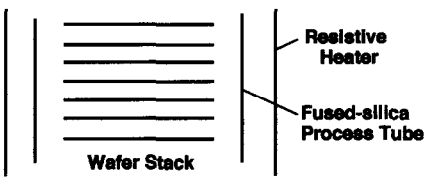
A	surface area
C	specific heat of silicon
F	view factor
J	radiosity
k	thermal conductivity
N	total number of surface elements
Q	heat flux
r	radial distance
R	radius of wafer
S	spacing between wafers
t	time
T	temperature
$\dot{T}_h$	heater temperature ramp rate
ΔT	temperature difference between the center and the edge of a wafer.

Greek symbols

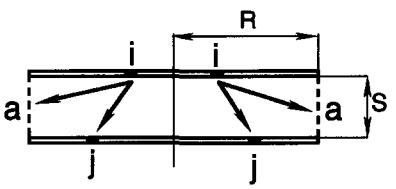
α	weighting factor defined in equation (16)
β	parameter defined in equation (18)
δ	wafer thickness
ε	emissivity
ρ	density
σ	Stefan–Boltzmann constant.

Subscripts

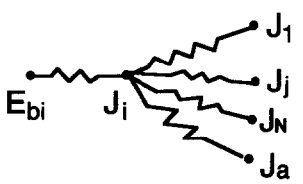
a	imaginary surface enclosing a unit cell as indicated in Fig. 1(b)
c	center of a wafer
e	edge of a wafer
h	heater
i, j	surface elements
t	process tube
w	wafer.



(a) Schematic diagram of a vertical batch thermal reactor



(b) Unit cell formed by two adjacent wafers



(c) Radiation network

Fig. 1. Thermal modeling of a batch thermal reactor.

wafers [Fig. 1(b)], which are considered to be part of an infinitely long wafer load in an infinitely long tube.

Since the reactor is axisymmetric and wafers are thin (0.7–0.8 mm), heat conduction in a wafer can be described as:

$$\rho C_p \frac{\partial T}{\partial t} = \frac{1}{r}\frac{\partial}{\partial r}\left(kr\frac{\partial T}{\partial r}\right) - 2q \tag{1}$$

where ρ, C_p, and k are the density, specific heat and thermal conductivity of silicon, respectively, and q represents the combined radiative and convective heat flux leaving a wafer surface per unit wafer thickness.

Badgwell *et al.* found experimentally that convective heat transfer is insignificant in low pressure CVD reactors [7, 8]. For atmospheric reactors, the ratio of convective and radiative heat transfer to the wafer stack can be estimated as:

$$\frac{\rho_g C_{p_g}(T_w - T_t)u}{\varepsilon^*\sigma(T_w^4 - T_h^4)} \tag{2}$$

where ρ_g and C_{pg} are the density and heat capacity of gases, respectively, u is the characteristic convective velocity, ε^* is the effective emissivity of the wafer stack, and T_w, T_t, and T_h are the wafer temperature, tube temperature and furnace heater temperature, respectively. Under typical reactor configuration and operating conditions, the ratio is less than 10% at temperatures higher than 600°C. As a result, convection is neglected in this work. This assumption is also justified by Hu [1] with a different method of analysis.

The boundary conditions are:

$$\frac{\partial T}{\partial r} = 0 \quad \text{at} \quad r = 0 \tag{3}$$

$$k\frac{\partial T}{\partial r}=\varepsilon_e(T_h^4-T_e^4) \quad \text{at} \quad r=R \tag{4}$$

where T_e and ε_e are the temperature and emissivity at wafer edge, respectively, and R is the wafer radius.

For the annular surface element i of area A_i [Fig. 1(b)], the next net radiative heat flux is:

$$Q_i=\frac{\varepsilon_i}{1-\varepsilon_i}(\sigma T_i^4-J_i)A_i \tag{5}$$

where σ is the Stefan–Boltzmann constant, J is the radiosity, and ε is the surface emissivity. For the outermost element ($i=N$), the edge of the wafer provides an additional surface for radiation:

$$Q_N=\frac{\varepsilon_N}{1-\varepsilon_N}A_N(\sigma T_N^4-J_N)+\pi R\delta\varepsilon_N\sigma(T_N^4-T_h^4) \tag{6}$$

where δ is the wafer thickness.

Near room temperature, radiation properties of silicon depend greatly on wavelength as well as temperature. Above 600°C, however, the emissivity of silicon is nearly constant at about 0.7 over a wavelength range from 0.7 to 15 μm [9, 10]. At relatively high temperatures, silicon wafers are also opaque [11, 12]. Siegel and Howell show that considering specular instead of diffuse surfaces only affects radiative energy transfer in enclosures slightly in many examples [13]. A comparison of experimental and analytical results also shows that regardless of the presence of specular surfaces, the diffuse-surface analysis agrees well with experimental results [14]. As a result, wafer surfaces can be treated to be gray, opaque and diffuse in batch reactor applications.

Radiation energy interchange between different elements can be evaluated by network theory [Fig. 1(c)]:

$$\frac{\sigma T_i^4-J_i}{\dfrac{1-\varepsilon_i}{\varepsilon_i}}=\sum_{j=1}^{N}F_{i,j}(J_i-J_j)+F_{i,a}(J_i-\sigma T_h^4) \tag{7}$$

where $F_{i,j}$ is the view factor from the surface element i to surface element j on the opposing wafer surface, and $F_{i,a}$ is the view factor from the surface element i to surface a. The view factor, $F_{i,j}$, can be obtained as:

$$F_{i,j}=F_{i,\Sigma j}-F_{i,\Sigma j-1} \quad (i,j=1,2,3,\ldots,N) \tag{8}$$

where $F_{i,\Sigma j}$ is the view factor from the element i to the sum of all the surfaces from the first up to the jth element, and $F_{i,\Sigma j}-1$ is that from the element i to the sum of all the surfaces from the first up to the $(j-1)$th element on the opposing wafer surface,

$$F_{i,\Sigma j}=(A_{\Sigma i}F_{\Sigma i,\Sigma j}-A_{\Sigma i-1}F_{\Sigma i-1,\Sigma j})/A_i, \tag{9}$$

$$F_{\Sigma i,\Sigma j}=0.5(w-(w^2-4v^2/u^2)^{0.5}), \tag{10}$$

$$u=r_i/S, v=r_j/S \quad \text{and} \quad w=1+(1+v^2)/u^2 \tag{11}$$

The view factor from the element i to the surface element a is:

$$F_{i,a}=1-\sum_{j=1}^{N}F_{i,j} \tag{12}$$

For a given furnace temperature ramp, $T_h(t)$, the transient wafer temperature $T(r,t)$ can be simulated. On the other hand, if maximum allowable wafer temperature nonuniformity is known, the process control parameter, $T_h(t)$, can be determined to ensure dislocation-free fabrication.

THERMAL CHARACTERISTICS

The general heat transfer model presented in the previous section is used in this work to investigate fundamental thermal characteristics of batch reactors. The coupled transient heat conduction and radiation equations are solved with the Cranck–Nicolson algorithm. The strong temperature dependence of the thermal conductivity of silicon is taken into account using the reported data [15].

Parabolic temperature distribution

Figure 2 represents typical radial temperature distributions on a wafer during furnace cooling under the three different control schemes: (1) a constant cooling rate ($\dot{T}_h$ = constant); (2) a constant temperature nonuniformity across the wafer (ΔT = constant); and (3) a constant ratio of thermal stress to yield stress ($\tau=1$). Near the wafer edge, large radiation view factors from the surface elements to the furnace surface result in efficient wafer cooling and steep temperature gradients. On the other hand, the center region is cooled mainly through heat conduction and wafer-to-wafer radiation since direct radiative energy exchange with the furnace surface is small. The normalized temperature distribution follows a universal profile and can be described excellently as:

$$\frac{T-T_c}{\Delta T}=-\left(\frac{r}{R}\right)^2 \quad \text{or} \quad \frac{T-T_e}{\Delta T}=1-\left(\frac{r}{R}\right)^2 \tag{13}$$

where T_c is the center wafer temperature and ΔT is the temperature difference between the center and the edge. Such distribution was also proposed by Huff and Goodall to evaluate thermal stresses [16]. Numerical simulations show that equation (13) is applicable during furnace cooling regardless of process conditions, i.e. wafer spacing, ramp rates and control schemes. The existence of this universal temperature profile has significant engineering implications. First, the thermal stress in wafers during furnace cooling should also follow a universal distribution, and the maximum stress is uniquely determined by ΔT. Second, only two parameters, ΔT and T_e (or T_c) are needed to describe the thermal state of the wafers. This feature is important for on-line process monitoring.

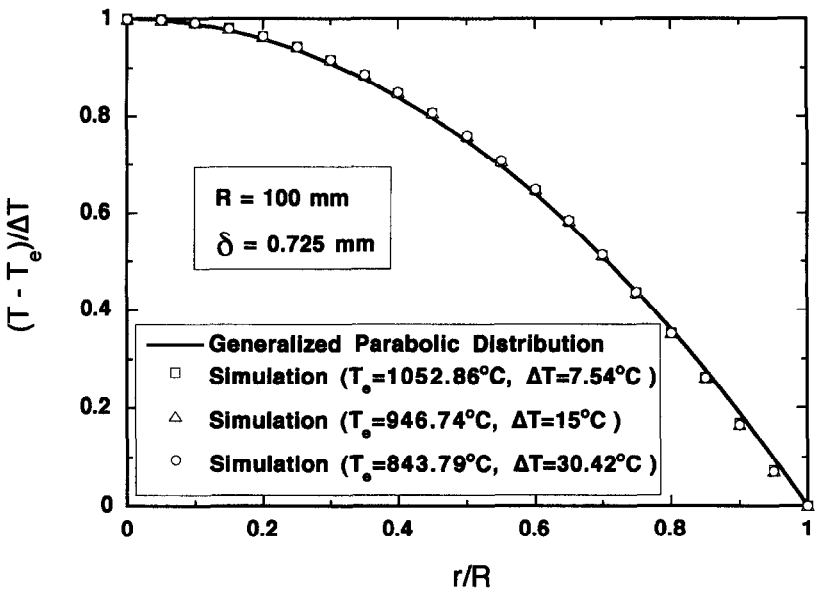


Fig. 2. Wafer temperature distribution (□, t = 400 s, S = 5 mm, constant ramp rate of 7.5°C min^{-1}; △, t = 280 s, S = 10 mm, constant $\triangle T$ of 15°C; ○, t = 210 s, S = 20 mm, τ = 1).

Cavity effect

The wafer stack in a batch thermal reactor forms radiation cavities. Radiation heat transfer between the wafer stack and the heater can be determined by an effective cavity emissivity, an apparent temperature, and the opening area. When the wafers are in thermal equilibrium, the radiative heat flux from a unit cell [Fig. 1(b)] to the heater is:

$$Q_a = 2\sum_i A_i F_{ia} J_i \tag{14}$$

and the effective emissivity of the wafer enclosure, ε_a, can be calculated as

$$\varepsilon_a = \frac{Q_a}{2\pi RS\sigma T_w^4} \tag{15}$$

where S is wafer spacing.

Figure 3 shows the effective emissivity of a unit cell formed by pure silicon wafers at high temperatures (ε_w = 0.7). The effective emissivity depends only on

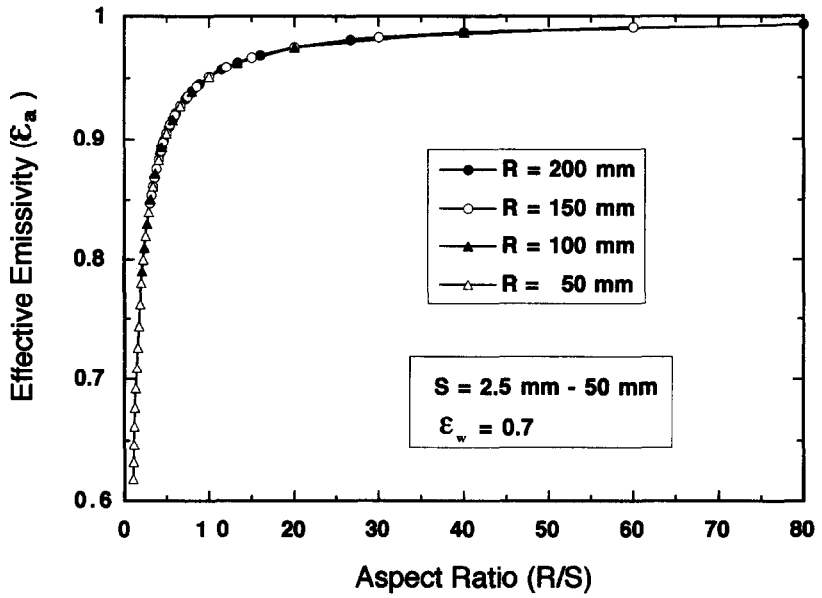


Fig. 3. Effective emissivity of a wafer enclosure.

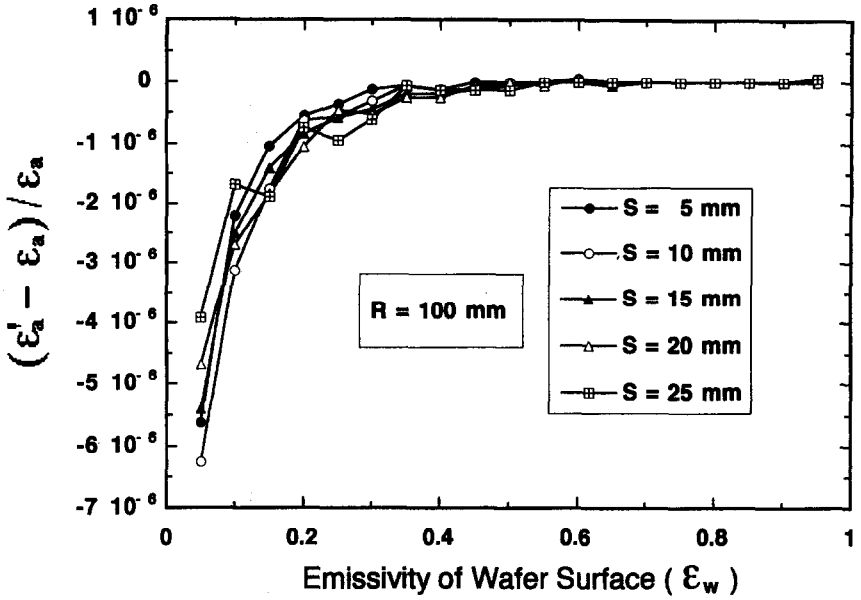


Fig. 4. Effect of wafer emissivity on the effective cavity emissivity.

the cavity aspect ratio (R/S). At relatively large aspect ratios (i.e. $R/S > 4$), the radiation cavity effect is significant. As the aspect ratio increases, the effective emissivity increases and approaches one.

During IC fabrication, the surface emissivity of the wafers can change greatly, i.e. from $\varepsilon_w = 0.1$ (metal films) to $\varepsilon_w = 0.9$ (oxides). Figure 4 shows the effect of water surface emissivity on the effective cavity emissivity. The results show that the difference between the effective emissivity of cavities formed by coated wafers (ε'_a) and those formed by pure silicon wafers (ε_a) is extremely small over a wide range of the cavity aspect ratios ($R/S = 4$–20). As a result, radiative energy transfer between wafer cavities and a reactor heater is independent of wafer emissivity, and a wafer stack can be represented by a cylindrical surface with an effective emissivity determined uniquely by the cavity aspect ratio (Fig. 3).

ENGINEERING MODEL

The universal temperature profile and the significant cavity effect of a wafer stack suggest that a simple yet accurate heat transfer model can be developed to link the critical process parameter (ΔT) directly to furnace configuration (R and S) and furnace operation (T_h), which is important for real-time process control to achieve defect-free fabrication. This model simplifies the wafer stack as a cylindrical surface of an effective emissivity ε_a (Fig. 3) and an apparent temperature T_a. The two unknown temperatures, ΔT and T_e (or T_c), can be determined by analyzing heat transfer between the wafer stack and the heater and within the wafer stack.

Apparent wafer-stack temperature

The apparent cavity temperature, T_a, is defined to represent the temperature of the enclosure formed by the wafers:

$$T_a = \left(\frac{Q_a}{2\pi RS\varepsilon_a\sigma}\right)^{1/4}. \tag{16}$$

It is the wafer temperature if the wafers are in thermal equilibrium. During transient cooling or heating, the cavity temperature is a weighted average of the center and edge temperatures:

$$T_a = \alpha T_c + (1-\alpha)T_e = T_e + \alpha\Delta T = T_c - (1-\alpha)\Delta T. \tag{17}$$

The weighting factor, α, can be evaluated from a parabolic temperature profile (ΔT and T_e), Q_a and the definition of T_a. This work has found that the dependence of α on ΔT is very weak and can be neglected. The weighting factor is mainly a geometric parameter (Fig. 5). In general, the cavity temperature is weighed towards the edge temperature. As the aspect ratio increases, T_a becomes closer to the edge temperature and α decreases.

Energy transfer between heater and wafer stack

Radiation heat transfer between the heater and the wafer stack can be simplified to that between the heater and the cylindrical surface:

$$\frac{d}{dt}\left(\int_0^R 2\pi r\delta\rho C_p T\,dr\right) = 2\pi RS\varepsilon_a\sigma[T_h^4 - (T_c - \alpha_1\Delta T)^4] + 2\pi R\delta\varepsilon_w\sigma[T_h^4 - (T_c - \Delta T)^4] \tag{18}$$

where $\alpha_1 = 1-\alpha$.

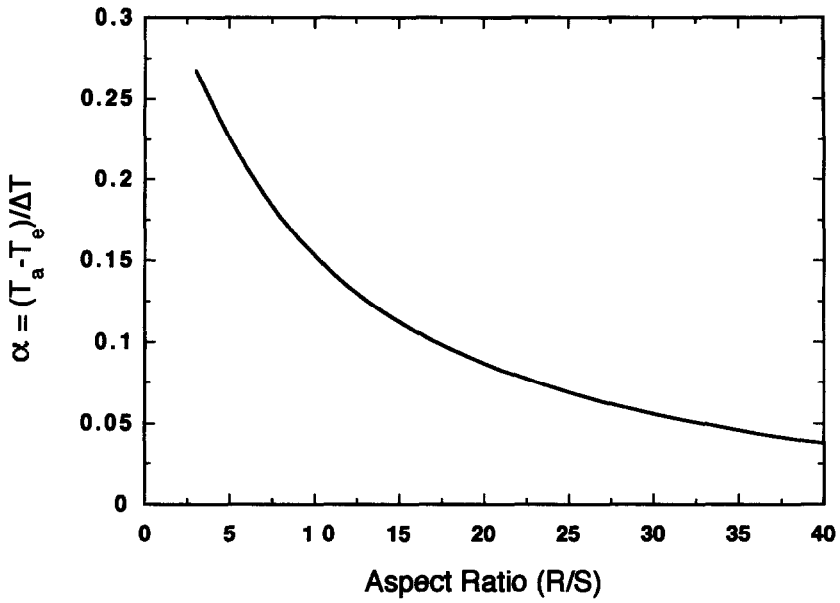


Fig. 5. Weighting factor α.

Since

$$\frac{dT_c}{dt} \gg \frac{d(\Delta T)}{dt},$$

equation (18) becomes:

$$\frac{dT_c}{dt} = \frac{2S\varepsilon_a\sigma[T_h^4-(T_c-\alpha_1\Delta T)^4]+2\delta\varepsilon_w\sigma[T_h^4-(T_c-\Delta T)^4]}{\delta\rho C_p R}. \quad (19)$$

Energy transfer inside a wafer stack

The energy equation for an infinitesimal disk element at the wafer center with a radius of r is:

$$\pi r^2\delta\rho C_p\frac{dT_c}{dt} = -2\pi r^2\frac{\varepsilon_w}{1-\varepsilon_w}(\sigma T_c^4 - J_c)+2\pi r\delta k\frac{dT}{dr} \quad (20)$$

where J_c is the radiosity of the central element.

Due to the radiation cavity effect, there exists a linear relationship between the normalized radiosity and the temperature difference:

$$\frac{J_c}{\sigma T_c^4} = 1-\beta\frac{1-\varepsilon_w}{\varepsilon_w}\frac{\Delta T}{T_c}. \quad (21)$$

The radiosity constant, β, is a geometric parameter when $R/S > 4$ and is independent of wafer emissivity (Fig. 6). Substituting equations (13) and (21) into equation (20) yields:

$$\frac{dT_c}{dt} = -\frac{4}{\rho C_p R^2}\left(k+\beta\sigma T_c^3\frac{R^2}{2\delta}\right)\Delta T. \quad (22)$$

This equation shows two significant results. First, the temperature nonuniformity is proportional to the change rate of the wafer temperature. Second, radiative transfer near the wafer center region can be viewed as a conduction process with an effective radiative conductivity:

$$k_r = \beta\sigma T_c^3\frac{R^2}{2\delta}. \quad (23)$$

At high temperatures, radiative energy transfer is the dominating mechanism to restore temperature uniformity on a wafer surface. For example, at 700°C, k_r is about 10 times k.

Equations (19) and (22) form a simple engineering model, which can be used to predict either the wafer temperature for a given furnace ramp, $T_h(t)$, or the required furnace ramp to achieve a desirable temperature nonuniformity, $\Delta T(T_c)$.

MODEL APPLICATIONS

Cooling of a batch furnace is often the most time-consuming process during thermal processing of silicon wafers such as oxidation and CVD deposition of thin films. A typical furnace ramp-down process takes about 2–3 h (cooling rate ~3–5°C min^{-1}). The next generation of microelectronics fabrication technology requires a significant reduction of furnace cooling time

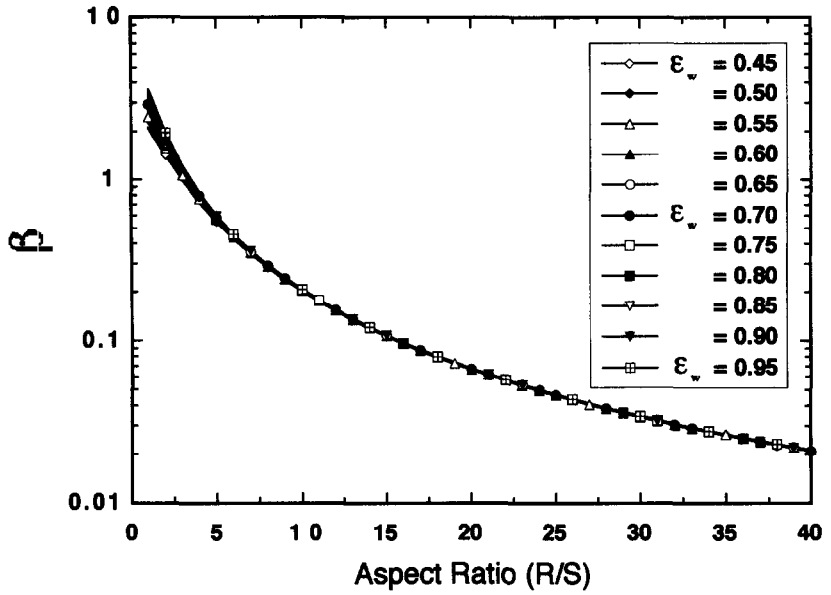


Fig. 6. Radiosity constant β.

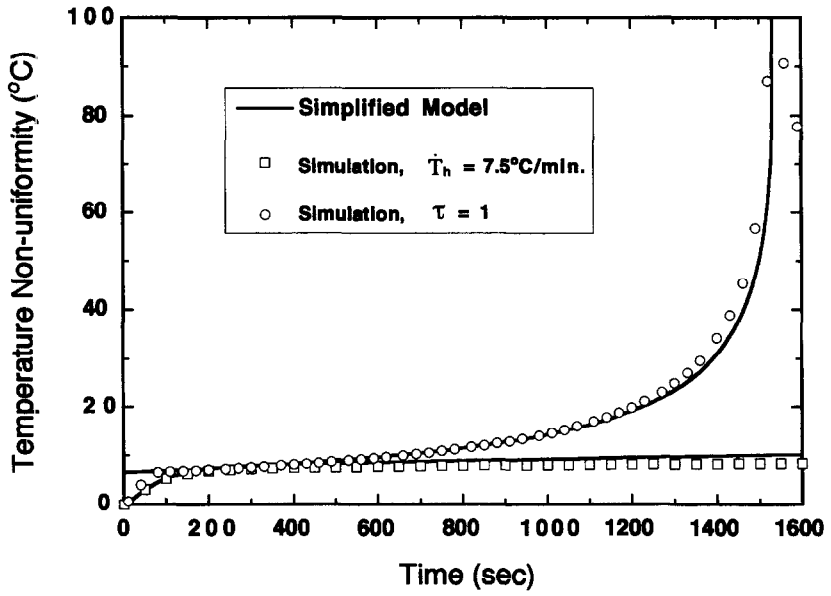


Fig. 7. Temperature nonuniformity during furnace ramp-down.

for two reasons: (1) to reduce the time a wafer exposed to high-temperature environment (thermal budget); and (2) to increase process efficiency. The highest achievable ramp rate is determined by the highest allowable thermal stress in silicon wafers [17]. To avoid defect generation, the maximum resolved shear stress, S_{max}, should not exceed the yield stress σ_y [16, 18–22].

Figures 7 and 8 represent predicted temperatures during a fast furnace ramp-down process from 1100 to 600°C for 200-mm diameter wafers. The wafer spacing is 5 mm and the thickness is 0.725 mm. Predictions based on the simple engineering model show excellent agreement with those based on the general heat transfer model. Under a constant cooling rate of 7.5°C min^{-1}, the wafer center-edge temperature difference, ΔT, increases rapidly during the initial 3 min and then increases very slightly during the next 60 min. The yield stress of silicon is small at high temperatures and large at relatively low temperatures. The most efficient control scheme is to use variable ramp rates so that the ratio of the maximum resolved shear stress to the critical stress remains one ($\tau = S_{max}/\sigma_y = 1$). By employing Haasen's model of the tem-

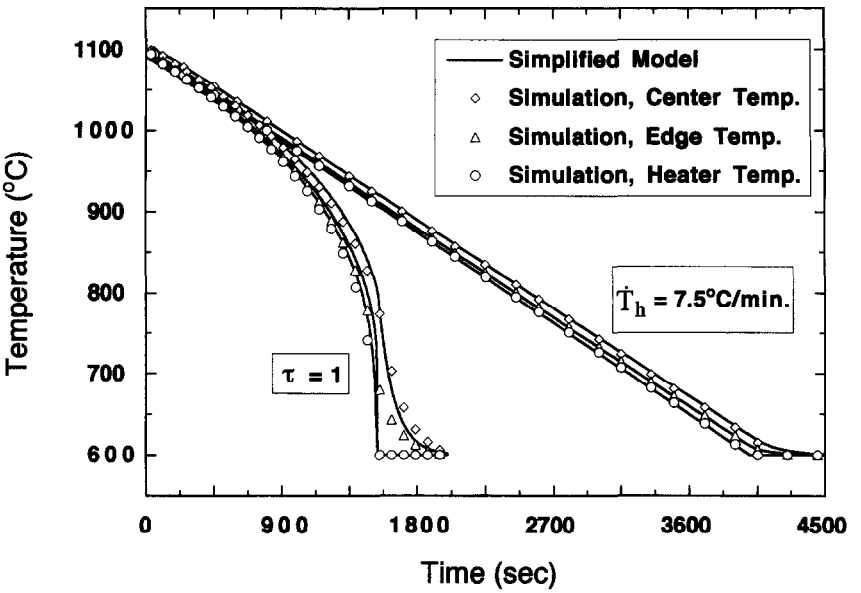


Fig. 8. Transient wafer and heater temperatures during fast furnace cooling.

perature dependence of the yield stress [21, 22], results of this work show that the wafer temperature uniformity must be controlled within 10°C during the initial 10 min of cooling from 1100°C (Fig. 7). After about 25 min, furnace ramp-down can be significantly accelerated. Figure 8 suggests that the stress-based control scheme can significantly reduce the wafer cooling time.

CONCLUSIONS

This work analyzes the fundamental features of thermal reactors during fast ramps. The transient wafer temperature distribution is shown to follow a universal parabolic profile over a wide range of process conditions, including process temperature, wafer spacing and control schemes. The radiation cavity effect is found to play a significant role in batch thermal reactors. Variations of wafer surface emissivity during process have negligibly small effect on the energy exchange between the heater and the wafers. A simple yet accurate engineering model is developed. The model shows that the wafer temperature nonuniformity is directly related to the furnace ramp rate, thermal conductivity of silicon and an equivalent radiative conductivity, and is independent of the wafer emissivity. This model is useful for real-time process control of fast-ramp and defect-free wafer processing.

Acknowledgement—Financial support for this work provided by Silicon Valley Group, Inc. is gratefully acknowledged.

REFERENCES

1. Hu, S. M., Temperature distribution and stresses in circular wafers in a row during radiative cooling. *Journal of Applied Physics*, 1969, **40,** 4413–4423.
2. Mokuya, K. and Matsuba, I., Characteristics of the transient wafer temperature distribution in a furnace for semiconductor fabrication processes. *Electronics and Communications in Japan*, Part 2, 1987, **70,** 59–65.
3. Mokuya, K., Matsuba, I. and Matsumoto, K., Transient model of wafer temperature in a furnace for semiconductor fabrication process. *Electronics and Communications in Japan*, Part 2, 1986, **69,** 1–11.
4. Van Schravendijk, B. J. and De Koning, W. L., Modeling and control of the wafer temperatures in a diffusion furnace. *Journal of Applied Physics*, 1987, **61,** 1620–1627.
5. Tavel, M. A. and Hearn, E. W., An interactive computer simulation of heating and cooling a row of silicon wafers. *Journal of the Electrochemical Society*, 1988, **135,** 1266–1271.
6. Fan, Y. H. and Qiu, T. W., Analyses of thermal stresses and control schemes for fast temperature ramps of batch furnaces. *IEEE Transactions on Semiconductor Manufacturing*, 1997, **10,** 433–437.
7. Badgwell, T. A., Edgar, T. F. and Trachtenberg, I., Experimental verification of a fundamental model for multi-wafer low pressure chemical vapor deposition of polysilicon. *Journal of the Electrochemical Society*, 1992, **139,** 524–532.
8. Badgwell, T. A., Edgar, T. F. and Trachtenberg, I., Modeling and scale-up of multi-wafer LPCVD reactors. *AIChE Journal*, 1992, **38,** 926–938.
9. Sato, T., Spectral emissivity in silicon. *Japanese Journal of Applied Physics*, 1967, **3,** 339–347.
10. Vandenabeele, P. and Maex, K., Emissivity of silicon wafers during rapid thermal processing. In *Rapid Thermal and Related Processing Techniques*, ed. R. Singh and M. Moslehi. SPIE, Santa Clara, CA, 1990, pp. 316–336.
11. Jellison, Jr, G. E. and Lowndes, D. H., Optical absorption coefficient of silicon at 1.152 μ at elevated temperature. *Applied Physics Letters*, 1982, **41,** 594–596.
12. Jellison, Jr, G. E., Optical and electrical properties of pulsed laser-annealed silicon. In *Semiconductors and Semimetal*, Vol. 23, ed. R. F. Wood and C. W. White. Academic Press, New York, 1984, pp. 95–163.
13. Siegel, R. and Howell, J. R., *Thermal Radiation Heat Transfer*, 2nd edn. McGraw-Hill, New York, 1981.
14. Schornhorst, J. R. and Viskanta, R., An experimental

examination of the validity of the commonly used methods of radiant heat transfer analysis. *Journal of Heat Transfer*, 1968, **90,** 429–436.
15. Touloukian, Y. S., Powell, P. W., Ho, C. Y. and Klemens, P. G., *Thermophysical Properties of Matter*, Vol. 1. IFI/Plenum, New York, 1970, p. 339.
16. Huff, H. R. and Goodall, R. K., Silicon wafer thermal processing: 300 mm issues. *Proceedings of the 2nd International Symposium on Advanced Science and Technology of Silicon Materials*, 1996, pp. 322–353.
17. Bentini, G., Correra, L. and Donolato, C., Defects introduced in silicon wafers during rapid isothermal annealing: thermoelastic and thermoplastic effects. *Journal of Applied Physics*, 1984, **56,** 2922–2929.
18. Schroter, W., Brion, H. G. and Siethoff, H., Yield point and dislocation mobility in silicon and germanium. *Journal of Applied Physics*, 1983, **54,** 1816–1920.
19. Yonenaga, I. and Sumino, K., Mechanical strength of silicon crystals as a function of the oxygen concentration. *Journal of Applied Physics*, 1984, **56,** 2346–2350.
20. Leroy, B. and Plougonven, C., Warpage of silicon wafers. *Journal of the Electrochemical Society*, 1980, **127,** 961–970.
21. Alexander, H. and Haasen, P., Dislocations and plastic flow in the diamond structure. *Solid State Physics*, 1968, **22,** 27–158.
22. Siethoff, H. and Haasen, P., Yield point and dislocation mobility in silicon. In *Lattice Defects in Semiconductors*, ed. R. R. Hasiguti. University of Tokyo, 1966, pp. 491–499.